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First Named Inventor	Welland, David R.
Group Art Unit	2816
Examiner Name	LE, DINH THANH
Attorney Docket Number	75622.P0016

ENCLOSURES ***(check all that apply)***

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  RESPONSE TO THE NOTICE OF NON-COMPLIANT APPEAL BRIEF

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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In Re Application of:
Welland et al.

Application No.: 09/686,072

Filed: October 11, 2000

Examiner: LE, DINH THANH

Group Art Unit: 2816

Attorney Docket No.: 75622.P0016

Title: METHOD AND APPARATUS FOR REDUCING INTERFERENCE

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RESPONSE TO THE NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the an interview with Examiner Le on March 21, 2007, Applicant respectfully submits this Summary of Claimed Subject Matter for the Appeal Brief submitted on June 15, 2005. As required by Examiner Le, paragraphs have been added to the end of section V, which map each independent claim to the Specification.

Respectfully submitted,

By _____
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V. Summary of Claimed Subject Matter

While it is highly desirable to integrate various components on a single integrated circuit for cost, size, power dissipation, and performance considerations, barriers to integration exist. In some circuits, one significant problem relates to interference between components in the integrated circuit.

The present invention provides several techniques for reducing interference in integrated circuits. The Specification describes several techniques for reducing interference including:

- Using fixed-value, non-programmable counters rather than programmable counters, as well as clocking at least one of the counters at a slower rate. As described below in detail, this technique reduces digital current in one part of an integrated circuit that causes spurious tones in another part of the integrated circuit. (See FIG. 4, Spec., page 14, line 13 to page 15, line 23; Claims 1, 66, 77, and 85).

- Reducing the mutual inductance between current loops in digital circuitry and current loops in other circuitry. In one example, supply filters are used to reduce the area of these loops. (See FIGS. 5-6, Spec., page 15, line 25 to page 18, line 15).

- Reducing the mutual inductance between current loops in the digital circuitry and current loops in other circuitry. In one example, conduits are used to reduce the area of the transmit loops by containing high frequency current flowing through a signal line which spans a relatively large distance. (See FIGS. 8-15, Spec., page 18, line 17 to page 21, line 25).

- Using a cancellation technique to reduce interference. For this technique, components of a circuit are arranged such that magnetic fields of certain components cancel the magnetic fields of other similar components. (See FIG. 16, Spec., page 22, lines 1-25).

- Managing the impedance of a circuit to reduce interference. In one example, replica circuitry is created and is controlled to always be in the opposite phase as the original circuitry. In this way, the impedance looking into the circuitry is approximately constant, independent of the state of the circuitry. (See FIGS. 17-18, Spec., page 22, line 17 to page 25, line 4).

- Containing leakage current in order to minimize the area of current loops. In one example, buffer circuits are used to confine leakage current within digital circuitry. (See FIGS. 19-23, Spec., page 25, line 6 to page 28, line 7).

- Using a filter at an integrated circuit clock input pin to reduce interference caused by a changing impedance at the clock input when the voltage of the clock input signal changes. (See FIG. 25, Spec., page 28, line 9 to page 29, line 14).

In two restriction requirements, the techniques listed above were restricted into seven groups. In the present patent application, the Applicants elected the first group listed above (using fixed-value, non-programmable counters rather than programmable counters), and the claims currently on appeal (claims 1, 52, 66, 77, and 85) relate to this technique (although Applicants submit that independent claim 52 is generic, and can also utilize any of the techniques listed above).

The first technique listed above reduces digital current (e.g., current from digital circuitry on an integrated circuit) in one part of an integrated circuit that causes spurious tones in another part of the integrated circuit. One major source of digital current that causes interference is divide-by-R counters, such as the divide-by-R counter 104 shown in FIG. 1. In typical prior art systems, divide-by-R counters are implemented using synchronous programmable counters. One problem with synchronous programmable counters is that the counter will have a large number of components. Another problem with synchronous programmable counters is that every flip-flop in the counter is clocked at the same speed. These problems result in interference. (Spec., page 14, lines 13-21).

The present invention reduces the digital current caused by divide-by-R counters by reducing the number of components in the divide-by-R counter. This is accomplished by using one or more fixed-value, non-programmable counters instead of programmable counters (see claim 1, lines 5-8; claim 66 lines 3-6; claim 77 lines 5-9; claim 85 lines 4-7), and clocking at least one of the counters at a slower rate (see claim 85 lines 8-9). (Spec., page 14, lines 21-24).

FIG. 1 is a block diagram illustrating a circuit having dividers 104 and 108. FIG. 4 is a similar block diagram, with the divide-by-R counter 104 replaced with two fixed-value, non-programmable counters 204 and 205. (Spec., page 15, lines 1-3). This arrangement results in less digital current, and thus less interference with other circuitry on an integrated circuit.

Following are independent claims 1, 52, 66, 77, and 85, each mapped to the Specification:

1. A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and *(Spec., page 15, lines 1-3; Figures 1, 4)*

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL, wherein the first and second fixed-value dividers are configured to divide by respective first and second fixed non-programmable division factors. *(Spec., page 14, lines 21-24; Figure 4)*

52. A method of integrating PLL circuitry for a wireless communication system onto a single integrated circuit, comprising the steps of:

forming the integrated circuit having PLL circuitry integrated on the integrated circuit, the PLL circuitry including VCO circuitry; and *(Spec., page 10, lines 2-6)*

applying one or more techniques to reduce interference present near the frequency of an output signal of the VCO circuitry. *(Spec., page 14, lines 4-11)*

66. A method of reducing interference in a circuit formed on an integrated circuit that includes a divider circuit, the method comprising the steps of:

providing a first fixed-value divider having an input and an output, wherein the first fixed-value divider is configured to divide by a first fixed non-programmable division factor; *(Spec., page 14, lines 21-24); (Spec., page 15, lines 1-7; Figure 4)*

providing a second fixed-value divider having an input and an output, wherein the second fixed-value divider is configured to divide by a second fixed non-programmable division factor; *(Spec., page 14, lines 21-24); (Spec., page 15, lines 1-7; Figure 4)*

coupling the output of the first fixed-value divider to the input of the second fixed-value divider; *(Spec., page 15, lines 1-7; Figure 4)*

coupling the output of the second fixed-value divider to the circuit; *(Spec., page 15, lines 1-7; Figure 4)*

generating a first output signal by applying an input frequency to the input of the first fixed-value divider to divide the input frequency by a first fixed value; and *(Spec., page 15, lines 1-10; Figure 4)*

generating a second output signal by applying the first output signal to the input of the second fixed-value divider to further divide the input frequency by a second fixed value. *(Spec., page 15, lines 1-10; Figure 4)*

77. A circuit for reducing interference on an integrated circuit comprising:

circuitry formed on the integrated circuit having an input; and

a divider formed on the integrated circuit and coupled to the input of the circuitry, wherein the divider further comprises:

a first fixed-value non-programmable divider for receiving an input signal and dividing the input signal by a first fixed amount, and*(Spec., page 14, lines 21-24); (Spec., page 15, lines 1-7; Figure 4)*

a second fixed-value non-programmable divider for receiving the divided signal from the first fixed-value divider and further dividing the input signal by a second fixed amount. *(Spec., page 14, lines 21-24); (Spec., page 15, lines 1-7; Figure 4)*

85. A method of reducing interference in a circuit formed on an integrated circuit, the circuit having one or more dividers, the method comprising the steps of:

selecting a divider in the circuit;

minimizing the number of circuit components used by the selected divider by using a plurality of fixed-value dividers rather than one or more programmable dividers, wherein each of the plurality of fixed-value dividers is configured to divide by a respective fixed non-programmable division factor; and *(Spec., page 14, lines 21-24); (Spec., page 15, lines 1-7; Figure 4)*

clocking at least one of the plurality of fixed-value dividers at a lower frequency than other fixed-value dividers in the circuit. *(Spec., page 14, lines 21-24)*